

FIG. 1

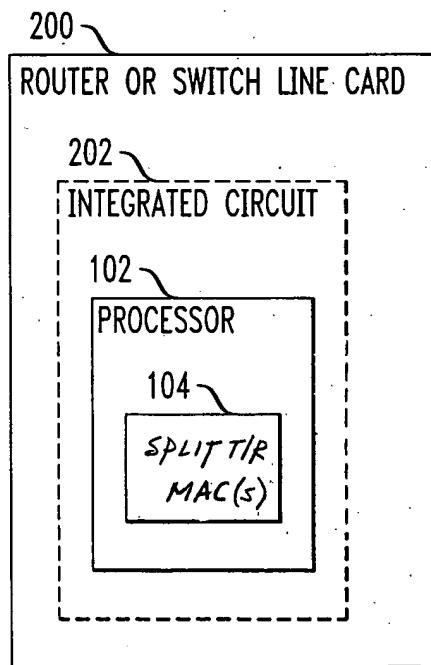


FIG. 2

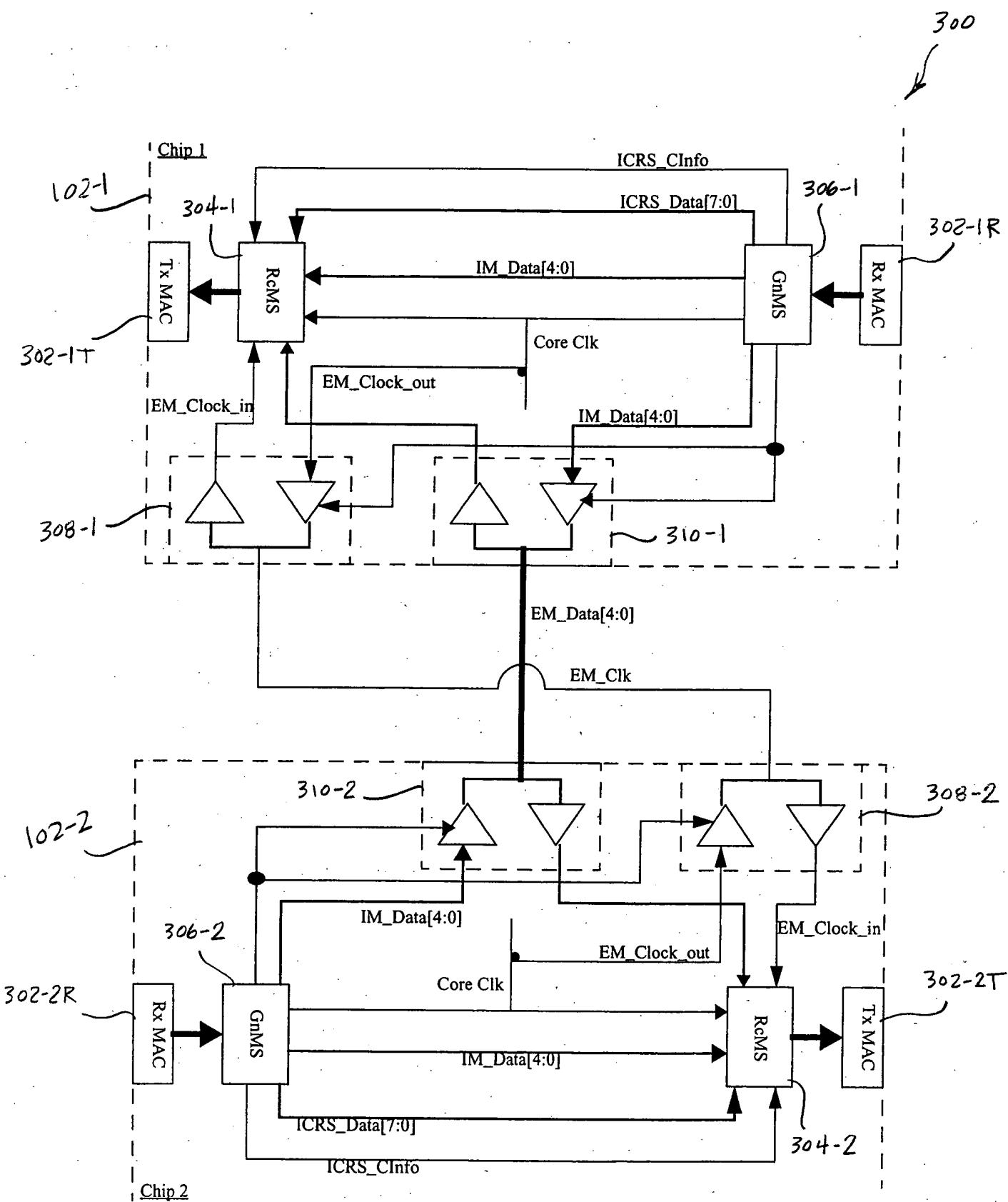


FIG. 3

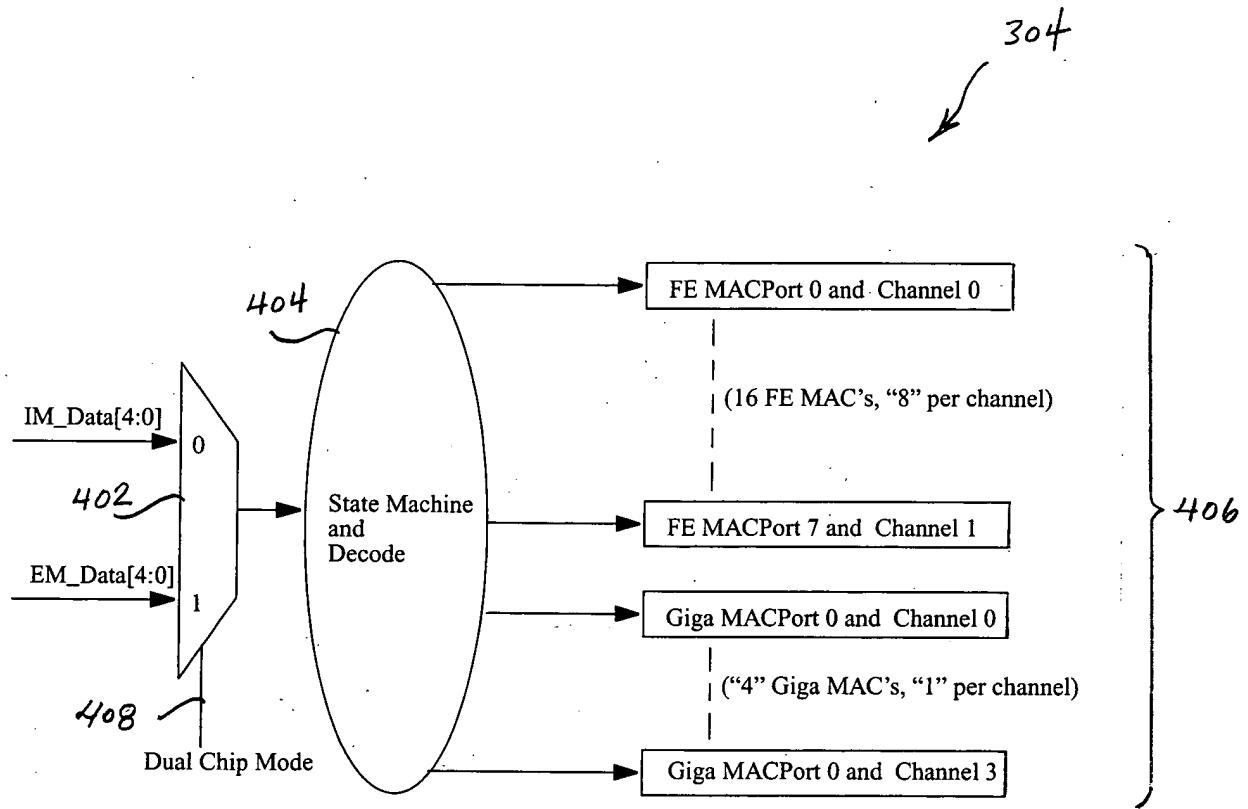
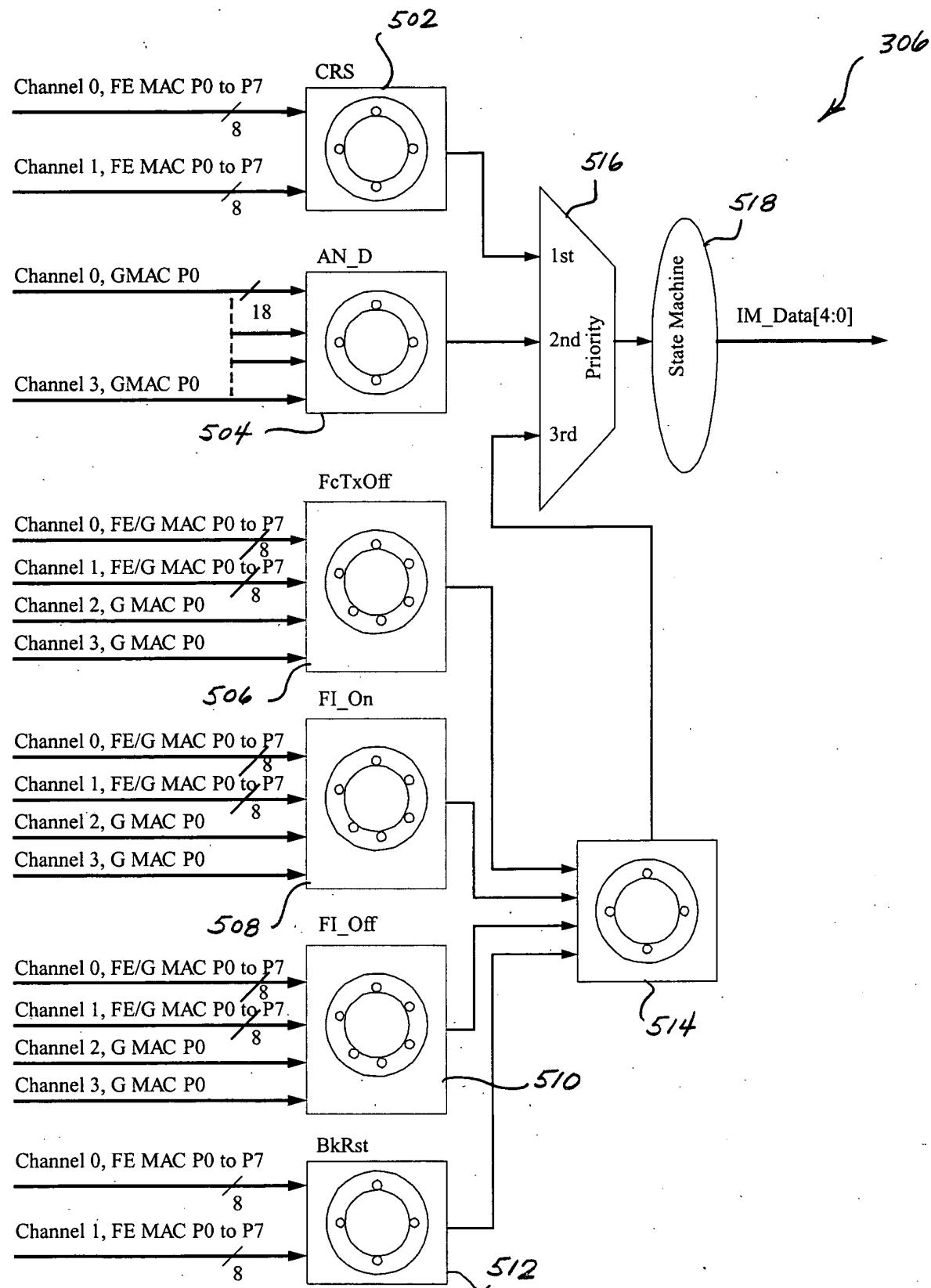


FIG. 4



FIG, 5

Addr decoding for CRS for FE MAC RX

Channel Addr[1:0]	Nib- ble Addr	[3:0]	Bit 0	Bit 1	Bit 2	Bit 3
00	0	CRS_C00_s	CRS_C0P0_s	CRS_C0P1_s	CRS_C0P2_s	CRS_C0P3_s
00	1	CRS_C01_s	CRS_C0P4_s	CRS_C0P5_s	CRS_C0P6_s	CRS_C0P7_s
01	0	CRS_C10_s	CRS_C1P0_s	CRS_C1P1_s	CRS_C1P2_s	CRS_C1P3_s
01	1	CRS_C11_s	CRS_C1P4_s	CRS_C1P5_s	CRS_C1P6_s	CRS_C1P7_s
10	0	CRS_C20_s	CRS_C2P0_s	CRS_C2P1_s	CRS_C2P2_s	CRS_C2P3_s
10	1	CRS_C21_s	CRS_C2P4_s	CRS_C2P5_s	CRS_C2P6_s	CRS_C2P7_s
11	0	CRS_C30_s	CRS_C3P0_s	CRS_C3P1_s	CRS_C3P2_s	CRS_C3P3_s
11	1	CRS_C31_s	CRS_C3P4_s	CRS_C3P5_s	CRS_C3P6_s	CRS_C3P7_s

FIG. 6

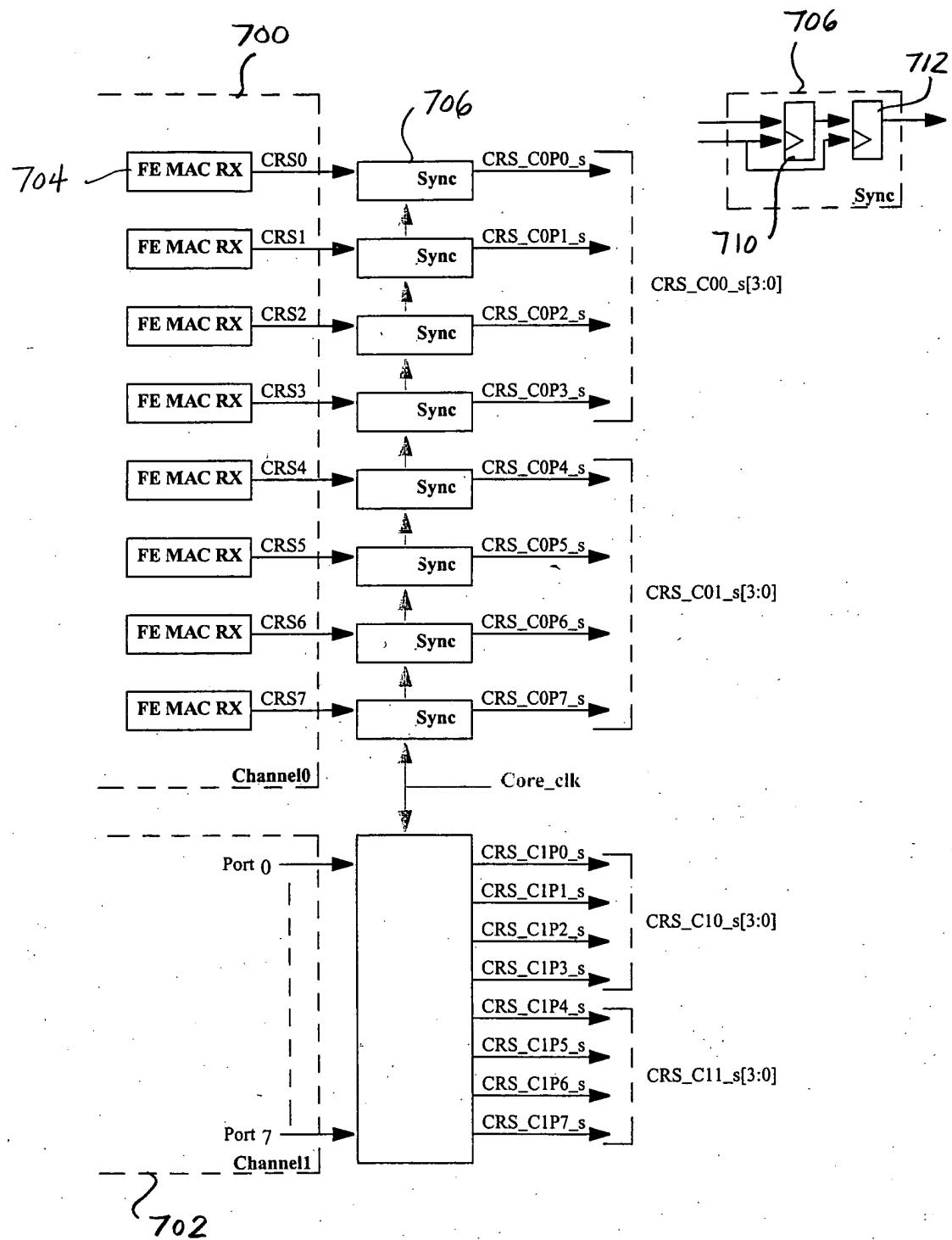


FIG. 7

Addr decoding for BkRst for 16 FE MAC RX

Channel Addr[1:0]	Nib- ble Addr	[3:0]	Bit 0	Bit 1	Bit 2	Bit 3
00	0	BkRst_C00_s	BkRst_C0P0_s	BkRst_C0P1_s	BkRst_C0P2_s	BkRst_C0P3_s
00	1	BkRst_C01_s	BkRst_C0P4_s	BkRst_C0P5_s	BkRst_C0P6_s	BkRst_C0P7_s
01	0	BkRst_C10_s	BkRst_C1P0_s	BkRst_C1P1_s	BkRst_C1P2_s	BkRst_C1P3_s
01	1	BkRst_C11_s	BkRst_C1P4_s	BkRst_C1P5_s	BkRst_C1P6_s	BkRst_C1P7_s
1X	NA	NA	NA	NA	NA	NA

FIG. 8

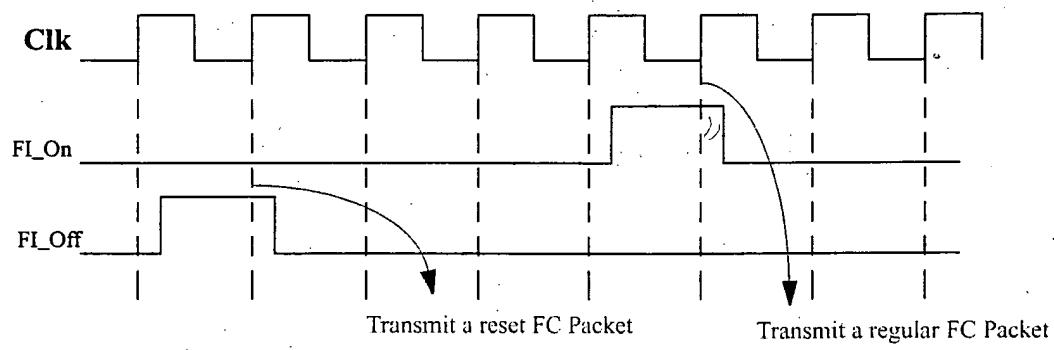


FIG. 9

Addr decoder for A-N register information

Channel Addr[1:0]	Nib- ble Addr/ Ctrl	[3:0]	Bit 0	Bit 1	Bit 2	Bit 3
00, 01, 10, 11	0, 1	AN_D0_s	TxLreg_s[0]	TxLreg_s[1]	TxLreg_s[2]	TxLreg_s[3]
	XDat a_s	AN_D1_s	TxLreg_s[4]	TxLreg_s[5]	TxLreg_s[6]	TxLreg_s[7]
	Xcon fig_s	AN_D2_s	TxLreg_s[8]	TxLreg_s[9]	TxLreg_s[10]	TxLreg_s[11]
	0	AN_D3_s	TxLreg_s[12]	TxLreg_s[13]	TxLreg_s[14]	TxLreg_s[15]

FIG. 10

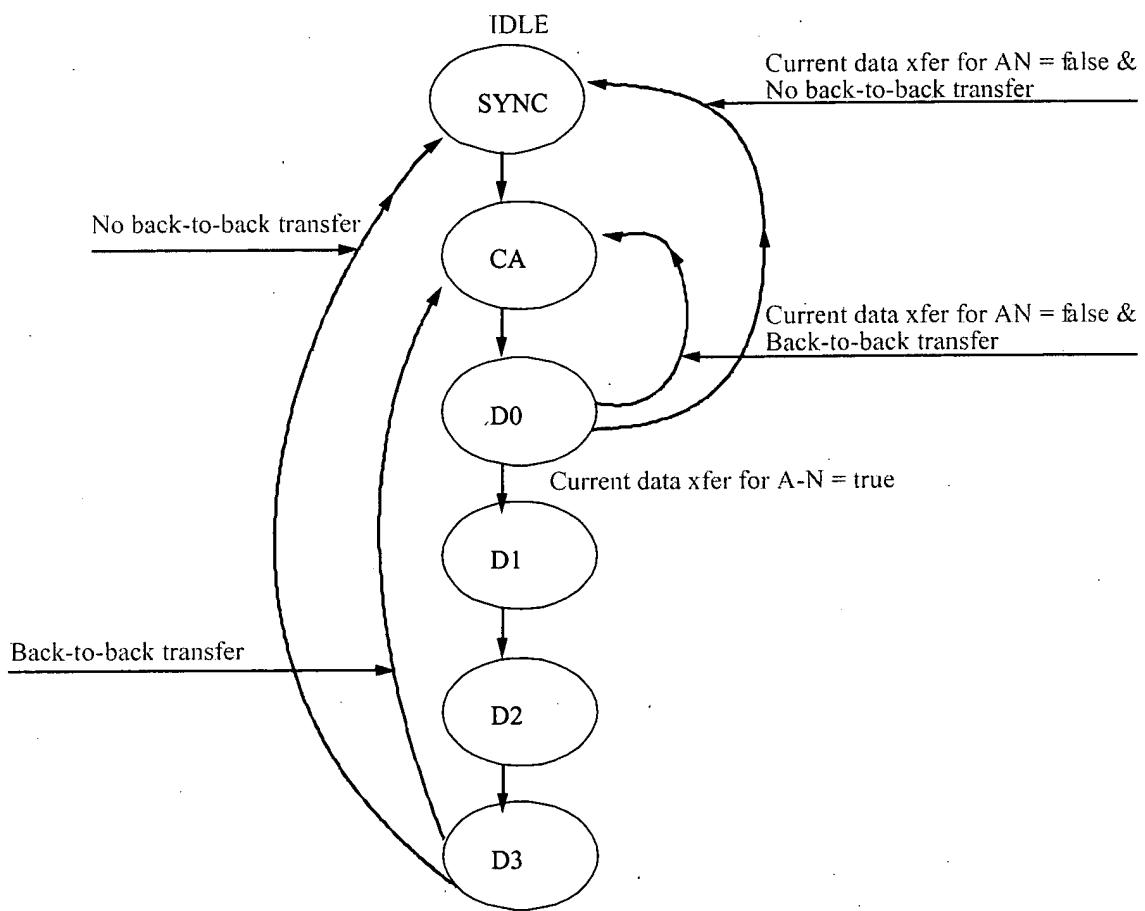


FIG. 11

**Control
Information Decode**

Ctrl[2:0]	Control Type
3'b000	SYNC
3'b001	CRS
3'b010	AN_D
3'b011	FcTxOFF
3'b100	FI_On
3'b101	FI_Off
3'b110	BkRst
3'b111	Reserved

FIG. 12

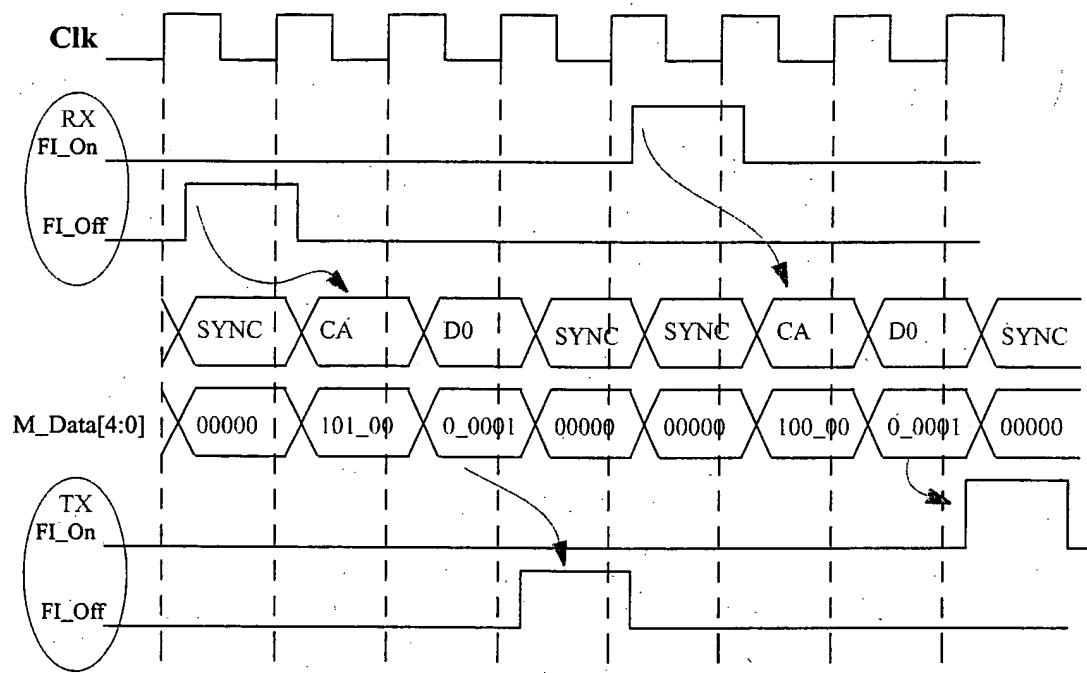


FIG. 13

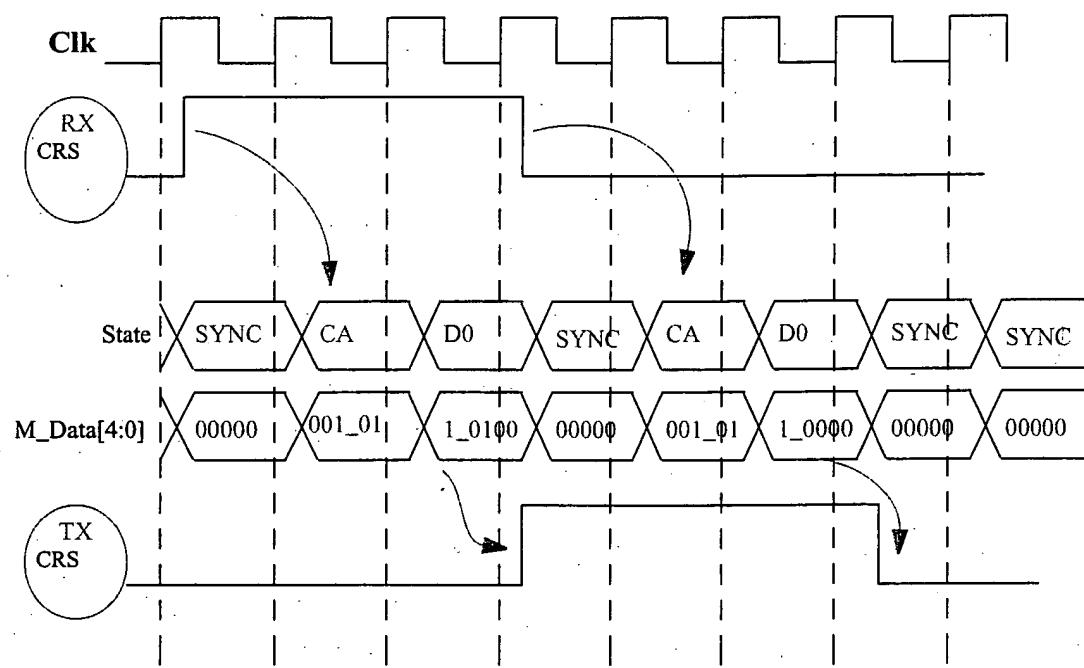


Fig. 14

Example waveform *FOR T/R INTERFACE*

<i>Clock</i>	x+1	x+2	x+3	x+4	x+5
<i>M_Data[4:0]</i>	5'b001_00	5'b0_1010	5'b101_10	5'b0_0001	5'b000_00
Phase	CA	Data	CA	Data	SYNC
Decoded Ctrl	CRS	NA	FI_Off	NA	NA
Channel Addr	Channel0	NA	Channel2	NA	NA
Nibble A/C	NA	0	NA	NA	NA
Data[3:0]	NA	4'b1010	NA	4'b0001	NA
		CRS_C00_s		FO_C20_s	

FIG. 15

Example for A-N info on T/R Interface for Channel 3, Nib address 0

<i>Clock</i>	x+1	x+2	x+3	x+4	x+5	x+6
<i>M_Data[4:0]</i>	5'b010_11	5'b0_1010	5'b1_0010	5'b0_1110	5'b0_1101	5'b000_00
Phase	CA	Data	Data	Data	Data	SYNC
Decoded Ctrl	A-N	NA	NA	NA	NA	NA
Channel Addr	Channel3	NA	NA	NA	NA	NA
Nibble A/C	NA	0	XData_s	XConfig_s	0	NA
Data[3:0]	NA	4'b1010	4'b0010	4'b1110	4'b1101	NA
		AN_D0_s	AN_D1_s	AN_D2_s	AN_D3_s	

FIG. 16